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Amendments to the Claims

Please add new claims 22-29 as follows:

1-11. (Cancelled)

12. (Previously Presented) A metal line structure formed in a semiconductor device, comprising:

first metal lines formed on a substrate, the first metal lines having a first barrier metal layer and a first conductive layer;

a first interlayer insulator between adjacent ones of the first metal lines;

second metal lines formed on respective ones of the first metal lines, the second metal lines having a second barrier metal layer and a second conductive layer; and

a second interlayer insulator between adjacent ones of the second metal lines;

wherein the first conductive layer is formed of a material different from that of the second conductive layer, and the first metal lines prevent ions of the second metal lines from being diffused into the substrate.

13. (Currently Amended) A metal line structure as defined in claim 12, wherein the first metal lines ~~has~~ have a thickness substantially identical to that of the second metal lines.

14. (Currently Amended) A metal line structure as defined in claim 12, wherein the first conductive layer ~~is formed of~~ comprises an Al alloy containing not greater than 5% Cu.

15. (Previously Presented) A metal line structure as defined in claim 12, wherein the first interlayer insulator has a thickness substantially identical to that of the second interlayer insulator.

16. (Currently Amended) A metal line structure as defined in claim 12, wherein the second conductive layer ~~is~~ consists essentially ~~formed~~ of Cu.

17. (Currently Amended) A metal line structure as defined in claim 12, wherein the first interlayer insulator ~~is made of~~ comprises undoped silicate glass (USG) or fluorinated silicate glass (FSG) deposited by an high density plasma (HDP) process.

18. (Previously Presented) A metal line structure as defined in claim 12, wherein the second interlayer insulator is made of undoped silicate glass (USG) or fluorinated silicate glass (FSG) deposited by a plasma enhanced chemical vapor deposition (PECVD) process.

19. (Previously Presented) A metal line structure as defined in claim 12, wherein the second interlayer insulator is made of undoped silicate glass (USG), fluorinated silicate glass (FSG) or SiOC deposited by a plasma enhanced chemical vapor deposition (PECVD) process.

20. (Original) A metal line structure as defined in claim 12, wherein the first and the second barrier metal layers comprise at least one of Ti, TiN, Ta, TaN, W and WN.

21. (Cancelled)

22. (New) A metal line structure as defined in claim 12, wherein the first interlayer insulator comprises undoped silicate glass (USG) or fluorinated silicate glass (FSG).

23. (New) A metal line structure as defined in claim 12, wherein the second interlayer insulator comprises undoped silicate glass (USG), fluorinated silicate glass (FSG) or SiOC.

24. (New) A metal line structure as defined in claim 12, wherein the second interlayer insulator comprises undoped silicate glass (USG) or fluorinated silicate glass (FSG).

25. (New) A metal line structure as defined in claim 12, wherein the first barrier metal layer comprises Ti.

26. (New) A metal line structure as defined in claim 12, wherein the first barrier metal layer comprises TiN.

27. (New) A metal line structure as defined in claim 12, wherein the second barrier metal layer comprises Ta.

28. (New) A metal line structure as defined in claim 12, wherein the second barrier metal layer comprises TaN.

29. (New) A structure in a semiconductor device, comprising:

first metal lines on a substrate configured to prevent ions of overlying second metal lines from diffusing into the substrate, the first metal lines having a first barrier metal layer and a first conductive layer comprising an Al alloy containing not greater than 5% Cu;

a first interlayer insulator between adjacent first metal lines;

second metal lines on the first metal lines, the second metal lines having a second barrier metal layer and a second conductive layer consisting essentially of Cu; and

a second interlayer insulator between adjacent second metal lines.